

REMARKS

In response to the Final Office Action mailed January 19, 2006, Applicants respectfully request reconsideration. Claims 1-32 were previously pending in this application. No claims have been added, amended, or canceled. As a result, claims 1-32 are pending for examination with claims 1 and 13 being independent claims. No new matter has been added.

Rejections Under 35 U.S.C. §103(a)

The Office Action rejected claims 1-32 under 35 U.S.C. §103(a) as being unpatentable over Pollachek (U.S. Pat. No. 4,648,074) in view of Lee et al. (U.S. Pat. No. 5,909,405), Garni et al. (U.S. Pat. No. 6,621,729) and Pasotti et al. (U.S. Pat. No. 6,535,428). Applicants respectfully traverse this rejection.

I. Discussion of Cited References

Pollachek is directed to a reference circuit with semiconductor memory array (Title). FIG. 3 illustrates a memory stack that forms a data storage portion of memory array 30 (col. 3, lines 43-45). A bit line of the memory stack is connected to one input of differential amplifier 22, which is used for reading the contents of the memory stack (col. 3, lines 55-56). Before the memory stack is read, the bit line is precharged to V_{DD} volts by applying a "precharge pulse (PC) to the gate electrode of PT1 which turns PT1 on momentarily" (col. 3, lines 61-64). Thus, transistor PT1 is not a load transistor, but merely a switching transistor that momentarily turns on prior to read-out to charge the bit line to the voltage V_{DD} so that the contents of the memory stack can be read (col. 5, lines 52-64).

Lee et al. is directed to a nonvolatile semiconductor memory (Title). As stated in the Office Action, Lee et al. refers to NAND-typed cell arrays as read only nonvolatile memories (col. 1, lines 11-14).

Applicants respectfully disagree that there exists motivation to combine Pollachek, Lee et al., Garni et al. and Pasotti et al. Although the lack of motivation will not be discussed further herein, Applicants reserve the right to raise this issue at a later date. The Garni et al. and Pasotti et al. references will not be discussed further herein because these references have been used to reject

dependent claims, but not an independent claim in the present application. Since independent claims 1 and 13 patentably distinguish over Pollachek and Lee et al. either alone or in combination (as will be discussed in further detail below), the dependent claims 2-12 and 14-32 are therefore patentable for at least the same reasons as the independent claims.

II. Even if the Combination of Pollachek and Lee et al. is Proper, the Claims Distinguish over the Combination

As discussed above, Pollachek illustrates two precharge transistors, PT1 and PTR, that are turned on momentarily to charge the bit lines prior to readout of the memory.

By contrast, claim 1 recites, *inter alia*, a first load for connection between a supply terminal and an input terminal of an output comparator, said first load being connected to said reference cell, and a second load, connectable to a nonvolatile memory cell, said first load and said second load each having a controllable resistance. Neither Pollachek nor Lee et al. teaches or suggests a load having a controllable resistance. Rather, as discussed above, Pollachek merely describes transistors, PT1 and PTR, which are switching transistors that turn on momentarily to charge bit lines to the supply level V_{DD} . Therefore, claim 1 patentably distinguishes over Pollachek and Lee et al. either alone or in combination. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 2-12 depend from claim 1 and are therefore patentable for at least the same reasons.

Claim 13 recites, *inter alia*, a control circuit coupled to a control input of the first transistor and the first conducting terminal of the first transistor such that the control circuit applies a control voltage to the control input that is substantially independent of a voltage difference between a voltage of the first conducting terminal and the supply voltage. Neither Pollachek nor Lee et al. teaches or suggests a control circuit coupled to control input of the first transistor and the first conducting terminal of the first transistor such that the control circuit applies a control voltage to the control input that is substantially independent of a voltage difference between a voltage of the first conducting terminal and the supply voltage. In fact, it does not appear that either Pollachek or Lee et al. teaches or suggests any control circuit whatsoever. Therefore, claim 13 patentably distinguishes over Pollachek or Lee et al. either alone or in combination. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 14-32 depend from claim 13 and are therefore patentable for at least the same reasons.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: May 18, 2006

Respectfully submitted,

By 

James H. Morris

Registration No.: 34,681

WOLF, GREENFIELD & SACKS, P.C.

Federal Reserve Plaza

600 Atlantic Avenue

Boston, Massachusetts 02210-2206

(617) 646-8000